REFERENCES

1. A. Dimoulas, G. Mavrou, G. Vellianitis, E. Evangelou, N. Boukos, M. Houssa, and M. Caymax, "HfO2 high-κ gate dielectrics on Ge (100) by atomic oxygen beam deposition," Appl. Phys. Lett., Volume No: 86, no. 3, pp. 032908, Jan. 2005.
2. A. Ford, J. Ho, Y. Chueh, Y. Tseng, Z. Fan, J. Guo, J. Bokor, and A. Javey, "Diameter-dependent electron mobility of InAs nanowires", Nano Letters, Volume No: 9, pp. 360-365, 2009.
3. A. Kerber, E. Cartier, G. Groeseneken, H. E. Maes, and U. Schwalke, "Stress induced charge trapping effects in SiO2/Al2O3 gate stacks with TiN electrodes," J. Appl. Phys., Volume No: 94, no. 10, pp. 6627–6630, Nov. 2003.
4. A. Rahman et al., "Theory of ballistic nanotransistors", IEEE Transaction on Electron Devices, Volume No: 50, pp. 1853-1864, 2003.
5. A.Pethe, T.Krishnamohan, D.Kim, S.Oh, H.S.P.Wong, and K.Saraswat (2005), "Investigation of the performance limits of III-V double-gate n-MOSFETs", Electron Devices Meeting, IEDM Technical Digest. IEEE International, pp.605-608.
6. Alain Nouailhat (2008), "An Introduction to Nanoscience and Nanotechnology", John Wiley & Sons, Inc., ISBN 978-1-84821-007-3.
7. Anurag Chaudhry and M. Jagadesh Kumar (2004), "Investigation of the Novel Attributes of a Fully Depleted Dual-Material Gate SOI MOSFET", IEEE Transactions on Electron Devices, Volume No. 51, Issue No. 9, pp: 1463-1467.
8. C. Chui, H. Kim, P. C. McIntyre, and K. Saraswat, "Atomic layer deposition of high-k dielectric for germanium MOS applications-substrate surface preparation," IEEE Electron Device Lett., Volume No: 25, no. 5, pp. 274–276, May 2004.
9. C. Jeong et al., "On backscattering and mobility in nanoscale silicon MOSFETs", IEEE IEDM, Volume No: 56, pp. 2762–2769, 2009.
10. C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400 ◦C germanium MOSFET technology with high-k dielectric and metal gate," in IEDM Tech. Dig., 2002, pp. 437–440.
11. C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-k gate dielectric," IEEE Electron Device Lett., Volume No: 23, no. 8, pp. 473–475, Aug. 2002.
12. C. Thelander et al., "Nanowire-based one dimensional electronics", Materials Today, Volume No: 9, pp. 28-35, 2006.

13. C. Thelander, L. Froberg, C. Rehnstedt, L. Samuelson, and L. Wernersson, “Vertical enhancement mode InAs nanowire field effect transistor with 50 nm wrap gate”, IEEE Electron Device Letters, Volume No: 29, pp. 206-208, 2008.
14. D. flandre et al., “Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits”, Microelectronics Laboratory, Belgium, Volume No: 21, pp. 213-228, 1999.
15. D. H. Kim and J. Del Alamo, “30-nm InAs PHEMTs With fT = 644 GHz and fmax = 681 GHz”, IEEE Electron Device Letters, Volume No: 31, pp. 806-808, 2010.
16. D. H. Kim, J. D. Alamo, D. Antoniadis, and B. Brar, “Extraction of virtual-source injection velocity in sub-100 nm III–V HFETs”, IEEE IEDM, pp. 1-4, 2009.
17. D. Kim et al., “Extraction of virtual-source injection velocity in sub-100 nm III–V HFETs”, IEEE IEDM, pp. 861–864, 2009.
18. D. Misra, R. Garg, P. Srinivasan, N. Rahim, and N. A. Chowdhury,0 “Interface characterization of high-k dielectrics on Ge substrates”, Materials Science and Semiconductor Processing, Volume No: 9, pp. 741, 2006.
19. E. H. Nicollian and J. J. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology. Hoboken, NJ: Wiley, 2003, p. 114.
20. Esmat Rafiee and Farzin Emami (2016), “Design and Analysis of a Novel Hexagonal Shaped Channel Drop Filter Based on Two-Dimensional Photonic Crystals”, Journal of Optoelectronical Nanostructures, Volume No.1, Issue No.2, pp: 39-46.
21. G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasaarathy, E. Vincent, and G. Ghibaudo, “Review on high-k dielectrics reliability issues,” IEEE Trans. Device Mater. Rel., Volume No: 5, no. 1, pp. 5–19, Mar. 2005.
22. G. Timp, J. Bude, et al., “The ballistic nanotransistors”, IEDM Tech Digest, pp. 55, 1999.
23. H. C. Casey, Jr., Devices For Integrated Circuit: Silicon and III–V Compound Semiconductors. Hoboken, NJ: Wiley, 1999, p. 310.
24. H. Ng, J. Han, T. Yamada, P. Nguyen, Y. Chen, and M. Meyyappan, Nano Letters, Volume No: 4, pp. 1247, 2004.
25. H. Okumura, T. Akane, and S. Matsumoto, “Carbon contamination free Ge(100) surface cleaning for MBE,” Appl. Surf. Sci., Volume No: 125, no. 1, pp. 125–128, Jan. 1998.
26. H. Shang, H. Okorn-Schmidt, K. K. Chan, M. Copel, J. A. Ott, P. M. Kozlowski, S. E. Steen, S. A. Cordes, H.-S. P. Wong, E. C. Jones, and W. E. Haensch, “High mobility p-channel Ge MOSFETs with a thin Ge oxynitride gate dielectric,” in IEDM Tech. Dig., 2002, pp. 441–443.

27. http://hkn.eecs.berkeley.edu/~leland/coursework/phys250.pdf.
28. http://www.cambridgenanotech.com/cnpruploads/ALD%20Tutorial.pdf.
29. J. Chen, N. A. Bojarczuk, J. H. Shang, M. Copel, J. B. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al2O3 and HfO2 gate dieletrics on surface-nitrided Ge," IEEE Trans. Electron Devices, Volume No: 51, no. 9, pp. 1441–1447, Sep. 2004.
30. J. Gu, A. Neal and P. Ye, "Effects of (NH4) 2S passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors", Applied Physics Letters, Volume No: 99, pp. 152113, 2011.
31. J. H. Chen, N. Bojarczuk, J. Shang, M. Copel, J. Hannon, J. Karasinski, E. Preisler, S. K. Banerjee, and S. Guha, "Ultrathin Al2O3 and HfO2 gate dielectric on surface-nitrided Ge", IEEE Trans. Electron Devices, Volume No: 51, pp. 1441-1447, 2004.
32. J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. I. Bersuker, "The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies," J. Appl. Phys., Volume No: 97, no. 5, p. 053704, Mar. 2005.
33. K. A. Dick, K. Deppert, L. Samuelson, and W. Seifert, "Optimization of Au-assisted InAs nanowires grown by MOVPE", Journal of Crystal Growth, Volume No: 297, pp. 326-333, 2006.
34. K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor", Journal of Applied. Physics, Volume No: 76, pp. 4879-4890, 1994.
35. L. Kang, B. H. Lee,W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," IEEE Electron Device Lett., Volume No: 21, no. 4, pp. 181– 183, Apr. 2000.
36. Luisa Filipponi and Duncan Sutherland (2013), "Nanotechnologies – Principles, Applications, Implications and Hands-on Activities", European Commission - Nano Sciences and Nano Technologies, ISBN 978-92-79-21437-0, ISSN 1018-5593.
37. M. Caymax, S. Elshocht, M. Houssa, A. Delabie, T. Conard, M. Meuris, et al., "sSOI fabrication by wafer bonding and layer splitting of thin SiGe virtual substrates", Material Science Engeneering: B, Volume No: 135, pp. 256–260, 2006.
38. M. Fischetti et al (1991), "Monte carlo simulation of semiconductors of transport in technologically significant semiconductors of the diamond and zinc-blende structures - part II: submicron MOSFETs", IEEE Transactions on Electron Devices, Volume No. 38, Issue No.3, pp. 650-660.

39. M. Houssa, L. Pantisano, L. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, et.al (2006), “Electrical properties of high-κ gate dielectrics: challenges, current issues, and possible solutions”, Materials Science & Engineering: Reports, Volume No.51, pp: 37-85.
40. M. Michielis, D. Esseni, and F. Driussi, “Analytical models for the insight into the use of alternative channel materials in ballistic nano-MOSFETs”, IEEE Transactions on Electron Devices, Volume No: 54, pp. 115-123, 2007.